## AMENDMENTS IN THE CLAIMS

1. (currently amended) A high speed static multiplexer comprising:

a plurality of data inputs and at least one select input;

an output;

a high voltage rail and a low voltage rail;

a pull-up circuit coupled between said output and said high voltage rail and further coupled to said plurality of data inputs and said at least one select input, wherein said pull-up circuit generates a first logic state at said output in response to a selected data input having said first logic state, wherein said pull-up circuit includes a first-type transistor and a plurality of second-type transistors, each having a control node, and a first and second data node, wherein said second data node of each of said plurality of second-type transistors is coupled to the control node of said first-type transistor, said first data node of each of said plurality of second-type transistors is coupled to a respective one of said plurality of data inputs, and said control node of each of said plurality of second-type transistors is coupled to one of said at least one select input; and

a pull-down circuit coupled between said output and said low voltage rail and further coupled to receive said plurality of data inputs and said at least one select input, wherein said pull-down circuit generates a second logic state at said output in response to a selected data input having said second logic state.

2. (currently amended) The high speed static multiplexer of Claim 1, wherein ~~said pull-up circuit comprises~~:

said first-type transistor is a P-type transistor having a control node, and a first and second data node, coupled at said first data node to said output and at said second data node to said high voltage rail, wherein said P-type transistor exhibits signal swings less than said high voltage rail; and

said ~~a~~ plurality of second-type transistors are N-type transistors~~, each having a control node, and a first and second data node, wherein said second data node of each of said plurality of N-type transistors is coupled to a the control node of said P-type transistor, said first data node of each of said plurality of N-type transistors is coupled to a respective one of said plurality of data~~

~~inputs, and said control node of each of said plurality of N-type transistors is coupled to said at least one select input~~.

3. (currently amended) The high speed static multiplexer of Claim [[2]] 1, wherein said pull-down circuit comprises:

a plurality of sets of second~~N~~-type transistors, wherein each set includes a first and second transistor coupled in series, and further wherein said second transistor is coupled at its second data node to said low voltage rail and at its control node to one of said [[at]] plurality of data inputs, and wherein said first transistor is further coupled at its control node to one of said at least one select input and at its first data node to said first data node of said first[[P]]-type transistor.

4. (original) The high speed static multiplexer of Claim 1, wherein each of said plurality of inputs are coupled to a respective inverter.

5. (currently amended) A high-speed static multiplexer comprising:

~~at least two~~ a plurality of data inputs ~~circuits that each receive a respective data input~~;

at least one select input, wherein each of said at least one select input receives a respective select signal, and when multiple different select inputs are provided said different select inputs are orthogonal with respect to each other ;

an output; and

a plurality of transistors operationally coupled between said ~~at least two~~ plurality of data input~~s~~ ~~circuits~~ and said output, wherein said plurality of transistors include a first-type transistor and a plurality of sets of second-type transistors, specific ones of which are coupled to a respective one of said plurality of data inputs, wherein said plurality of transistors each have a control node and a first and second data node and wherein said plurality of data inputs and said at least one select input controls said plurality of sets of second-type transistors ~~are controlled by both data inputs and select signals~~ to select ~~of~~ one of said data inputs to yield said output;

wherein each set of said second-type transistors includes a first, second and a third transistor and the respective one of said plurality of data inputs is coupled to a control node of said third transistor and to a first data node of said first transistor; and one of said at least one

select input is coupled to a control node of said first transistor and to a control node of said second transistor.

6. (currently amended) The high speed static multiplexer of Claim 5, wherein said first-type ~~plurality of~~ transistor~~s include~~ is a P-type transistor and said second-type transistors are ~~a plurality of sets of first, second, and third~~ N-type transistors ~~for each of said at least two data inputs~~.

7. (currently amended) The high-speed static multiplexer of Claim 6, wherein each of said ~~at least two~~ plurality of data input~~s~~ ~~circuits~~ includes an in-line inverter for inverting each ~~said~~ respective data input to produce an inverted input.

8. (canceled)

9. (currently amended) The high speed static multiplexer of Claim [[8]] 6, wherein further:

a second data node of said first N-type transistor is connected to a control node of said P-type transistor;

a second data node of said P-type transistor is connected to a power supply (VDD); and

a first data node of said P-type transistor is connected to said output.

10. (original) The high speed static multiplexer of Claim 9, wherein further:

a second data node of said third N-type transistor is connected to ground;

a first data node of said third N-type transistor is coupled to a second data node of said second N-type transistor; and

a first data node of said second N-type transistor is coupled to said first data node of said P-type transistor at said output.

11. (original) The high speed static multiplexer of claim 6, wherein said P-type transistor has an on state and off state and wherein a voltage differential at said control node to change between said on and off states is less than the voltage differential between a high voltage

applied at a second data node of said P-type transistor and a low voltage applied at a second data node of said third N-type transistor.

12. (original) The high speed static multiplexer of claim 6, wherein said plurality of transistors are field effect transistors (FETs).

13. (currently amended) A multi-level high-speed static multiplexer comprising:

a plurality of connected levels of high speed static multiplexers, wherein each of said high speed multiplexers comprises:

a plurality of data inputs and at least one select input;

an output;

a high voltage rail and a low voltage rail;

a pull-up circuit coupled between said output and said high voltage rail and further coupled to said plurality of data inputs and said at least one select input, wherein said pull-up circuit generates a first logic state at said output in response to a selected data input having said first logic state, wherein further said pull-up circuit includes a first transistor and a plurality of second transistors, each having a control node, and a first and second data node, wherein said second data node of each of said plurality of second transistors is coupled to the control node of said first transistor, said first data node of each of said plurality of second transistors is coupled to a respective one of said plurality of data inputs, and said control node of each of said plurality of second transistors is coupled to one of said at least one select input; and

a pull-down circuit coupled between said output and said low voltage rail and further coupled to said plurality of data inputs and said at least one select input, wherein said pull-down circuit generates a second logic state at said output in response to a selected data input having said second logic state; and

wherein each of said outputs at a first level of said plurality of levels is coupled to one of said plurality of data inputs of said high speed static multiplexers at a next level of said plurality of levels, wherein a multiplicative-input multiplexer is realized having NxM possible outputs, where N is a number of data inputs at said first level and M is the number of data inputs at the next level.

13. (canceled)

14. (original) The multi-level high speed static multiplexer circuit of Claim 13, wherein each even number of levels yields a corrected output and each odd number of level yields an inverted output.

15. (original) The multi-level high speed static multiplexer of Claim 14, further comprising an inverter coupled to each of said data inputs at said first level when said number of levels is odd.

16. (original) The multi-level high speed static multiplexer of Claim 14, further comprising an inverter coupled to said output at said final level when said number of levels is odd.

17. (Newly added) The multi-level high speed static multiplexer of Claim 13, wherein:

said first transistor is a P-type transistor having a control node, and a first and second data node, coupled at said first data node to said output and at said second data node to said high voltage rail, wherein said P-type transistor exhibits signal swings less than said high voltage rail; and

said plurality of second transistors are N-type transistors.

18. (Newly added) The multi-level high speed static multiplexer of Claim 13, wherein said pull-down circuit comprises:

a plurality of sets of N-type transistors, wherein each set includes a first and second transistor coupled in series, and further wherein said second transistor is coupled at its second data node to said low voltage rail and at its control node to one of said plurality of data inputs,

and wherein said first transistor is further coupled at its control node to one of said at least one select input and at its first data node to said first data node of said first-type transistor.

19. (Newly added) The multi-level high speed static multiplexer of Claim 13, wherein:

said plurality of transistors each have a control node and a first and second data node and wherein said plurality of data inputs and said at least one select input controls said plurality of sets of second-type transistors to select one of said data inputs to yield said output;

wherein each set of said second-type transistors includes a first, second and a third transistor and a respective one of said plurality of data inputs is coupled to a control node of said third transistor and to a first data node of said first transistor; and said at least one select input is coupled to a control node of said first transistor and to a control node of said second transistor.

20. (Newly added) The multi-level high speed static multiplexer of Claim 12, wherein said plurality of levels includes more than two levels with a final level having a single high speed static multiplexer, and wherein each of said outputs of a given level is fed into at least one input at a next level until said final level.

21. (Newly added) The high speed static multiplexer of Claim 1, wherein:

said plurality of transistors each have a control node and a first and second data node and wherein said plurality of data inputs and said at least one select input controls said plurality of sets of second-type transistors to select one of said data inputs to yield said output;

wherein each set of said second-type transistors includes a first, second and a third transistor and a respective one of said plurality of data inputs is coupled to a control node of said third transistor and to a first data node of said first transistor; and said at least one select input is coupled to a control node of said first transistor and to a control node of said second transistor.

22. (Newly added) The high speed static multiplexer of Claim 20, wherein further:

a second data node of said first N-type transistor is connected to a control node of said P-type transistor;

a second data node of said P-type transistor is connected to a power supply (VDD);

a first data node of said P-type transistor is connected to said output.

a second data node of said third N-type transistor is connected to ground;

a first data node of said third N-type transistor is coupled to a second data node of said second N-type transistor; and

a first data node of said second N-type transistor is coupled to said first data node of said P-type transistor at said output.